

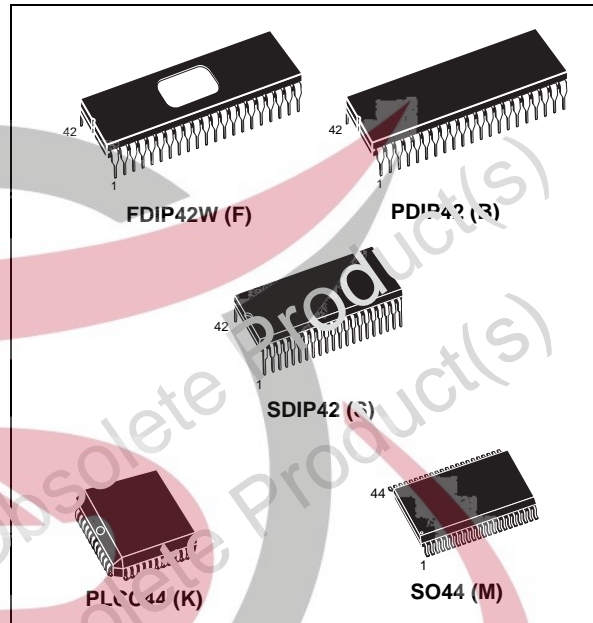


## M27C160

16 Mbit (2 Mb x 8 or 1 Mb x 16) UV EPROM and OTP EPROM

### Features

- 5V  $\pm$  10% Supply Voltage in Read Operation
- Access Time: 50 ns
- Byte-wide or Word-wide Configurable
- 16 Mbit Mask ROM Replacement
- Low Power Consumption
  - Active Current: 70 mA at 8 MHz
  - Standby Current: 100  $\mu$ A
- Programming Voltage: 12.5V  $\pm$  0.25V
- Programming Time: 50  $\mu$ s/word
- Electronic Signature
  - Manufacturer Code: 20h
  - Device Code: B1h
- ECOPACK® packages available



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# 1 Summary description

The M27C160 is a 16-Mbit EPROM offered in two ranges UV (Ultraviolet Erase) and OTP (One-Time Programmable). It is ideally suited for microprocessor systems requiring large data or program storage and is organized as either 2 Mbit words of 8 bits or 1 Mbit word of 16 bits. The pin-out is compatible with a 16-Mbit Mask ROM.

The FDIP42W (window ceramic frit-seal package) has a transparent lid which enables the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written rapidly to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C160 is offered in PDIP42, SDIP42, PLCC44 and SO44 packages.

In order to meet environmental requirements, ST offers the M27C160 in ECOPACK<sup>(®)</sup> packages. ECOPACK packages are Lead-free. The category of second Level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

See [Figure 1: Logic diagram](#) and [Table 1: Signal names](#) for a brief overview of the signals connected to this device.

**Figure 1. Logic diagram**

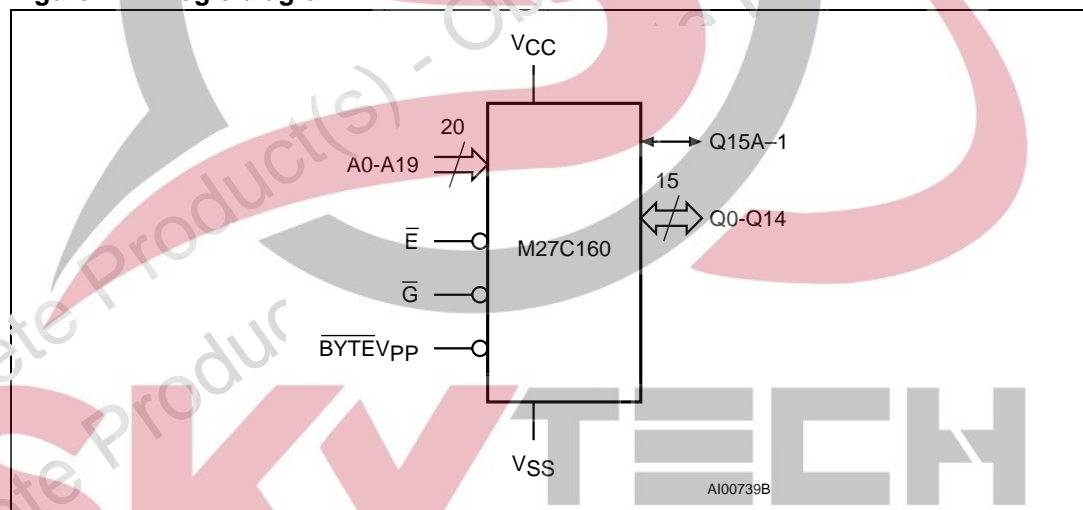


Table 1. Signal names

| Signal              | Description                 |
|---------------------|-----------------------------|
| A0-A19              | Address Inputs              |
| Q0-Q7               | Data Outputs                |
| Q8-Q14              | Data Outputs                |
| Q15A-1              | Data Output / Address Input |
| $\overline{E}$      | Chip Enable                 |
| $\overline{G}$      | Output Enable               |
| BYTEV <sub>PP</sub> | Byte Mode / Program Supply  |
| V <sub>CC</sub>     | Supply Voltage              |
| V <sub>SS</sub>     | Ground                      |
| NC                  | Not Connected Internally    |

Figure 2. PLCC Connections

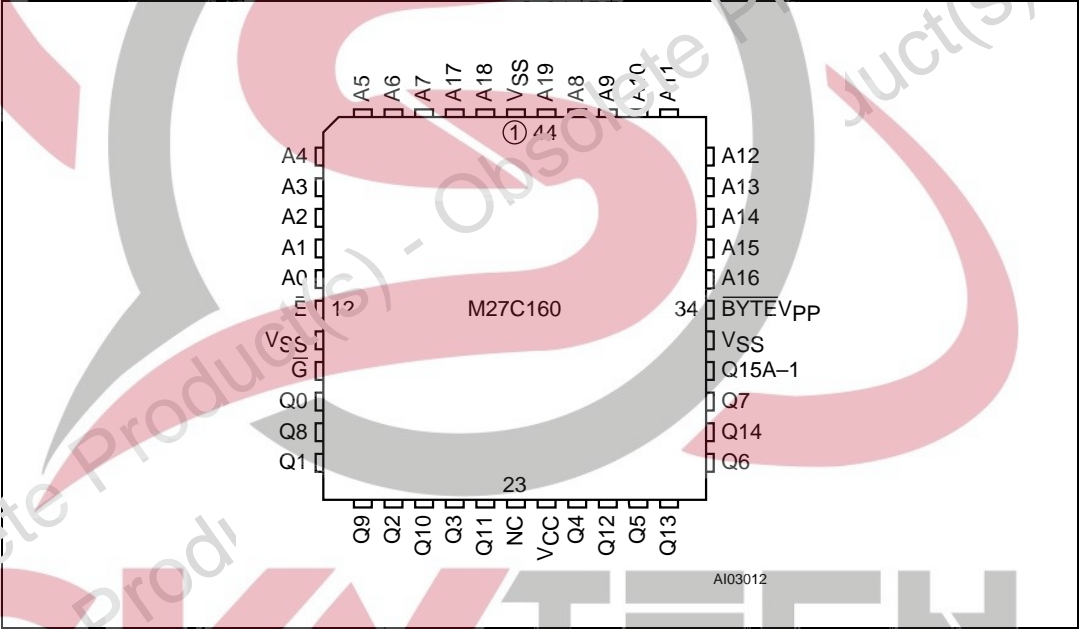




Figure 3. DIP Connections

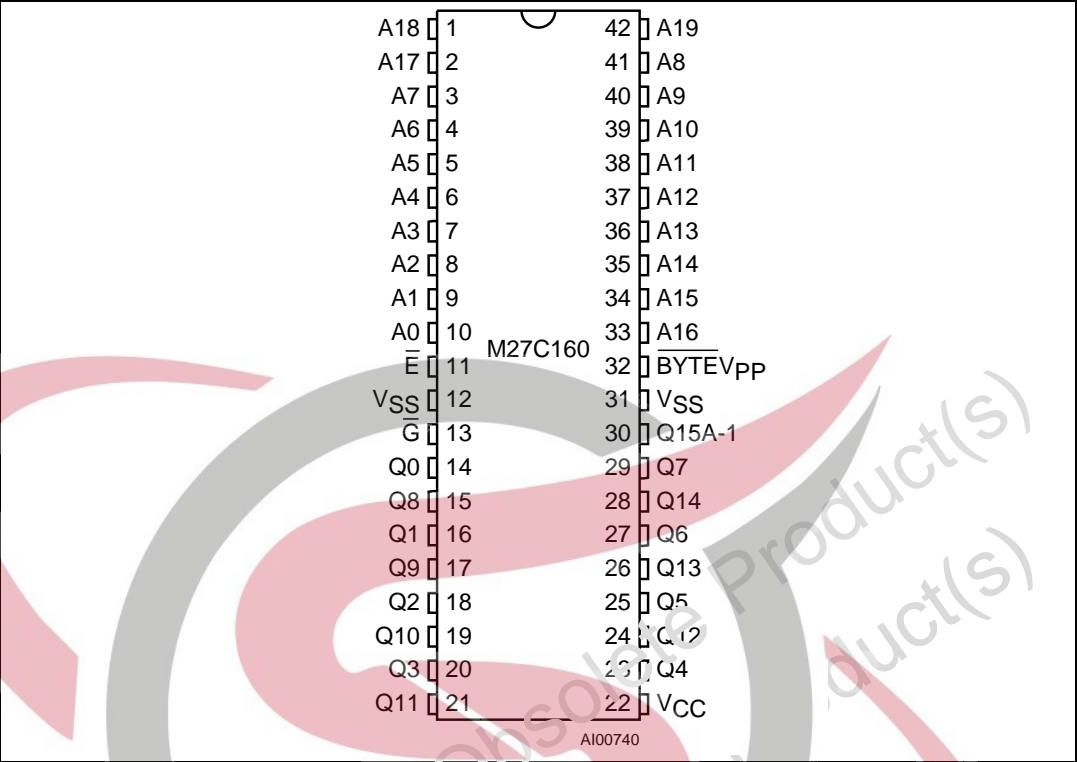
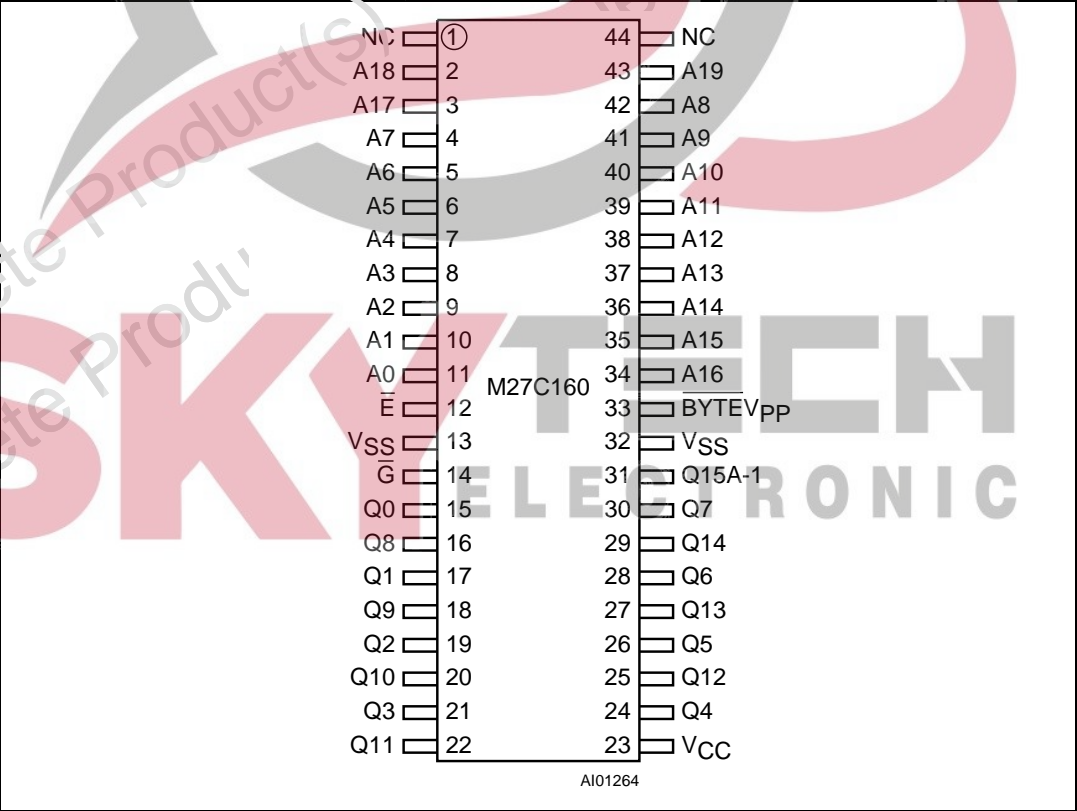


Figure 4. SO Connections



## 2 Device description

[Table 2](#) lists the operating modes of the M27C160. A single power supply is required in the read mode. All inputs are TTL compatible except for  $V_{PP}$  and 12V on A9 for the Electronic Signature.

**Table 2. Operating Modes**

| Mode                 | $\bar{E}$      | $\bar{G}$ | $\overline{BYTEV_{PP}}$ | A9       | Q15A-1   | Q8-Q14   | Q7-Q0    |
|----------------------|----------------|-----------|-------------------------|----------|----------|----------|----------|
| Read Word-wide       | $V_{IL}$       | $V_{IL}$  | $V_{IH}$                | X        | Data Out | Data Out | Data Out |
| Read Byte-wide Upper | $V_{IL}$       | $V_{IL}$  | $V_{IL}$                | X        | $V_{IH}$ | Hi-Z     | Data Out |
| Read Byte-wide Lower | $V_{IL}$       | $V_{IL}$  | $V_{IL}$                | X        | $V_{IL}$ | Hi-Z     | Data Out |
| Output Disable       | $V_{IL}$       | $V_{IH}$  | X                       | X        | Hi-Z     | Hi-Z     | Hi-Z     |
| Program              | $V_{IL}$ Pulse | $V_{IH}$  | $V_{PP}$                | X        | Data In  | Data In  | Data In  |
| Verify               | $V_{IH}$       | $V_{IL}$  | $V_{PP}$                | X        | Data Out | Data Out | Data Out |
| Program Inhibit      | $V_{IH}$       | $V_{IH}$  | $V_{PP}$                | X        | Hi-Z     | Hi-Z     | Hi-Z     |
| Standby              | $V_{IH}$       | X         | X                       | X        | Hi-Z     | Hi-Z     | Hi-Z     |
| Electronic Signature | $V_{IL}$       | $V_{IL}$  | $V_{IH}$                | $V_{ID}$ | Code     | Codes    | Codes    |

Note: X =  $V_{IH}$  or  $V_{IL}$ ,  $V_{ID} = 12V \pm 0.5V$ .

### 2.1 Read mode

The M27C160 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the  $\overline{BYTEV_{PP}}$  pin. When  $\overline{BYTEV_{PP}}$  is at  $V_{IH}$  the Word-wide organisation is selected and the Q15A-1 pin is used for Q15 Data Output. When the  $\overline{BYTEV_{PP}}$  pin is at  $V_{IL}$  the Byte-wide organisation is selected and the Q15A-1 pin is used for the Address Input A-1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A-1 at  $V_{IL}$  the lower 8 bits of the 16 bit data are selected and with A-1 at  $V_{IH}$  the upper 8 bits of the 16 bit data are selected.

The M27C160 has two control functions, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte-wide organisation must be selected.

Chip Enable ( $\bar{E}$ ) is the power control and should be used for device selection. Output Enable ( $\bar{G}$ ) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that the addresses are stable, the address access time ( $t_{AVQV}$ ) is equal to the delay from  $\bar{E}$  to output ( $t_{ELQV}$ ). Data is available at the output after a delay of  $t_{GLQV}$  from the falling edge of  $\bar{G}$ , assuming that  $\bar{E}$  has been low and the addresses have been stable for at least  $t_{AVQV} - t_{GLQV}$ .

### 2.2 Standby mode

The M27C160 has a standby mode which reduces the active current from 50mA to 100µA. The M27C160 is placed in the standby mode by applying a CMOS high signal to the  $\bar{E}$  input.



When in the standby mode, the outputs are in a high impedance state, independent of the  $\overline{G}$  input.

## 2.3 Two-line output control

Because EPROMs are usually used in larger memory arrays, this product features a 2-line control function which accommodates the use of multiple memory connection. The two line control function allows:

- the lowest possible memory power dissipation,
- complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines,  $\overline{E}$  should be decoded and used as the primary device selecting function, while  $\overline{G}$  should be made a common connection to all devices in the array and connected to the  $\overline{READ}$  line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

## 2.4 System considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the supplies to the devices. The supply current  $I_{CC}$  has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of  $\overline{E}$ .

The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device outputs. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1  $\mu$ F ceramic capacitor is used on every device between  $V_{CC}$  and  $V_{SS}$ . This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a 4.7  $\mu$ F electrolytic capacitor should be used between  $V_{CC}$  and  $V_{SS}$  for every eight devices.

This capacitor should be mounted near the power supply connection point. The purpose of this capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

## 2.5 Programming

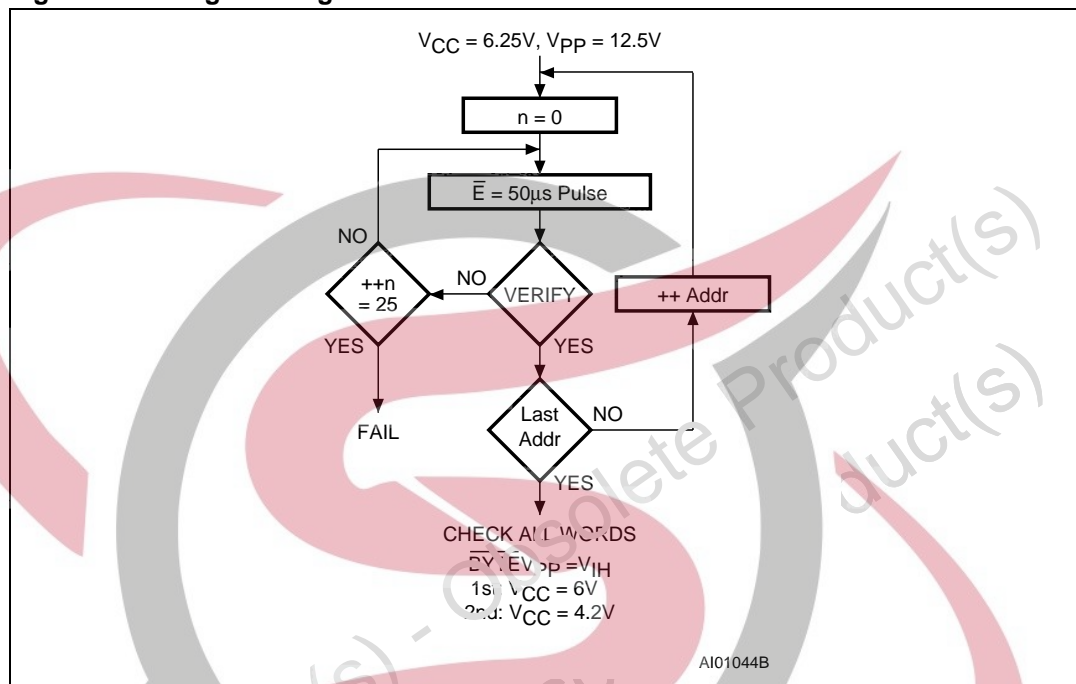
When delivered (and after each erasure for UV EPROM), all bits of the M27C160 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations. Although only '0's will be programmed, both '1's and '0's can be present in the data word. The only way to change a '0' to a '1' is by die exposure to ultraviolet light (UV EPROM). The M27C160 is in the programming mode when  $V_{PP}$  input is at 12.5V,  $\overline{G}$  is at  $V_{IH}$  and  $\overline{E}$  is pulsed to  $V_{IL}$ . The data to be programmed is applied to 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.  $V_{CC}$  is specified to be  $6.25V \pm 0.25V$ .

## 2.6 Presto III programming algorithm

The Presto III Programming Algorithm allows the whole array to be programmed with a guaranteed margin in a typical time of 52.5 seconds. Programming with Presto III consists of

applying a sequence of 50µs program pulses to each word until a correct verify occurs (see Figure 5). During programing and verify operation a Margin mode circuit is automatically activated to guarantee that each cell is programed with enough margin. No overprogram pulse is applied since the verify in Margin mode provides the necessary margin to each programmed cell.

**Figure 5. Programming Flowchart**



## 2.7 Program Inhibit

Programming of multiple M27C160s in parallel with different data is also easily accomplished. Except for  $\bar{E}$ , all like inputs including  $\bar{G}$  of the parallel M27C160 may be common. A TTL low level pulse applied to a M27C160's  $\bar{E}$  input and  $V_{PP}$  at 12.5V, will program that M27C160. A high level  $\bar{E}$  input inhibits the other M27C160s from being programmed.

## 2.8 Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with  $\bar{E}$  at  $V_{IH}$  and  $\bar{G}$  at  $V_{IL}$ ,  $V_{PP}$  at 12.5V and  $V_{CC}$  at 6.25V.

## 2.9 Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the  $25^{\circ}C \pm 5^{\circ}C$

ambient temperature range that is required when programming the M27C160. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C160, with  $V_{PP} = V_{CC} = 5V$ . Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from  $V_{IL}$  to  $V_{IH}$ . All other address lines must be held at  $V_{IL}$  during Electronic Signature mode. Byte 0 ( $A0 = V_{IL}$ ) represents the manufacturer code and byte 1 ( $A0 = V_{IH}$ ) the device identifier code. For the STMicroelectronics M27C160, these two identifier bytes are given in [Table 3](#) and can be read-out on outputs Q7 to Q0.

**Table 3. Electronic Signature**

| Identifier          | A0       | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Hex Data |
|---------------------|----------|----|----|----|----|----|----|----|----|----------|
| Manufacturer's Code | $V_{IL}$ | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 20h      |
| Device Code         | $V_{IH}$ | 1  | 0  | 1  | 1  | 0  | 0  | 0  | 1  | 21h      |

Note: Outputs Q15-Q8 are set to '0'.

## 2.10 Erasure operation (applies to UV EPROM)

The erasure characteristics of the M27C160 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C160 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C160 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C160 window to prevent unintentional erasure. The recommended erasure procedure for M27C160 is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 30 W-sec/cm<sup>2</sup>. The erasure time with this dosage is approximately 30 to 40 minutes using an ultraviolet lamp with 12000 µW/cm<sup>2</sup> power rating. The M27C160 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

### 3 Maximum ratings

**Table 4. Absolute Maximum Ratings <sup>(1)</sup>**

| Symbol                  | Parameter                                    | Value      | Unit |
|-------------------------|--|------------|------|
| $T_A$                   | Ambient Operating Temperature <sup>(2)</sup> | –40 to 125 | °C   |
| $T_{BIAS}$              | Temperature Under Bias                       | –50 to 125 | °C   |
| $T_{STG}$               | Storage Temperature                          | –65 to 150 | °C   |
| $V_{IO}$ <sup>(3)</sup> | Input or Output Voltage (except A9)          | –2 to 7    | V    |
| $V_{CC}$                | Supply Voltage                               | –2 to 7    | V    |
| $V_{A9}$ <sup>(3)</sup> | A9 Voltage                                   | –2 to 13.5 | V    |
| $V_{PP}$                | Program Supply Voltage                       | –2 to 14   | V    |

1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Depends on range.
3. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns.  
Maximum DC voltage on Output is  $V_{CC} + 0.5V$  with possible overshoot to  $V_{CC} + 2V$  for a period less than 20ns.



## 4 DC and AC characteristics

$T_A = 0$  to  $70\text{ }^{\circ}\text{C}$  or  $-40$  to  $85\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 5\text{V} \pm 5\%$  or  $5\text{V} \pm 10\%$ ;  $V_{PP} = V_{CC}$

**Table 5. Read Mode DC Characteristics <sup>(1)</sup>**

| Symbol         | Parameter                     | Test Condition  | Min. | Max.         | Unit          |
|----------------|-------------------------------|---|------|--------------|---------------|
| $I_{LI}$       | Input Leakage Current         | $0\text{V} \leq V_{IN} \leq V_{CC}$   |      | $\pm 1$      | $\mu\text{A}$ |
| $I_{LO}$       | Output Leakage Current        | $0\text{V} \leq V_{OUT} \leq V_{CC}$  |      | $\pm 10$     | $\mu\text{A}$ |
| $I_{CC}$       | Supply Current                | $\bar{E} = V_{IL}, \bar{G} = V_{IL}, I_{OUT} = 0\text{mA}, f = 8\text{MHz}$ |      | 70           | mA            |
|                |                               | $\bar{E} = V_{IL}, \bar{G} = V_{IL}, I_{OUT} = 0\text{mA}, f = 5\text{MHz}$ |      | 50           | mA            |
| $I_{CC1}$      | Supply Current (Standby) TTL  | $\bar{E} = V_{IH}$  |      | 1            | mA            |
| $I_{CC2}$      | Supply Current (Standby) CMOS | $\bar{E} > V_{CC} - 0.2\text{V}$  |      | 100          | $\mu\text{A}$ |
| $I_{PP}$       | Program Current               | $V_{PP} = V_{CC}$   |      | 10           | $\mu\text{A}$ |
| $V_{IL}$       | Input Low Voltage             |   | -0.3 | 0.8          | V             |
| $V_{IH}^{(2)}$ | Input High Voltage            |   | 2    | $V_{CC} + 1$ | V             |
| $V_{OL}$       | Output Low Voltage            | $I_{OL} = 2.1\text{mA}$   |      | 0.4          | V             |
| $V_{OH}$       | Output High Voltage TTL       | $I_{OH} = -400\mu\text{A}$  | 2.4  |              | V             |

1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

2. Maximum DC voltage on Output is  $V_{CC} + 0.5\text{V}$ .

$T_A = 25\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$ ;  $V_{PP} = 12.5\text{V} \pm 0.25\text{V}$

**Table 6. Programming Mode DC Characteristics <sup>(1)</sup>**

| Symbol   | Parameter               | Test Condition              | Min. | Max.           | Unit          |
|----------|-------------------------|-----------------------------|------|----------------|---------------|
| $I_{LI}$ | Input Leakage Current   | $0 \leq V_{IN} \leq V_{CC}$ |      | $\pm 1$        | $\mu\text{A}$ |
| $I_{CC}$ | Supply Current          |                             |      | 50             | mA            |
| $I_{PP}$ | Program Current         | $\bar{E} = V_{IL}$          |      | 50             | mA            |
| $V_{IL}$ | Input Low Voltage       |                             | -0.3 | 0.8            | V             |
| $V_{IH}$ | Input High Voltage      |                             | 2.4  | $V_{CC} + 0.5$ | V             |
| $V_{OL}$ | Output Low Voltage      | $I_{OL} = 2.1\text{mA}$     |      | 0.4            | V             |
| $V_{OH}$ | Output High Voltage TTL | $I_{OH} = -2.5\text{mA}$    | 3.5  |                | V             |
| $V_{ID}$ | A9 Voltage              |                             | 11.5 | 12.5           | V             |

1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .



Table 7. Capacitance <sup>(1)</sup>

| Symbol           | Parameter  | Test Condition        | Min. | Max. | Unit |
|------------------|--|-----------------------|------|------|------|
| C <sub>IN</sub>  | Input Capacitance (except $\overline{\text{BYTE}}V_{PP}$ ) | V <sub>IN</sub> = 0V  |      | 10   | pF   |
|                  | Input Capacitance ( $\overline{\text{BYTE}}V_{PP}$ )       | V <sub>IN</sub> = 0V  |      | 120  | pF   |
| C <sub>OUT</sub> | Output Capacitance   | V <sub>OUT</sub> = 0V |      | 12   | pF   |

1. Sampled only, not 100% tested.

T<sub>A</sub> = 25 °C, f = 1 MHz

Table 8. AC Measurement Conditions

| Parameter                             | High Speed | Standard     |
|---------------------------------------|------------|--------------|
| Input Rise and Fall Times             | ≤ 10ns     | ≤ 20ns       |
| Input Pulse Voltages                  | 0 to 3V    | 0.4V to 2.4V |
| Input and Output Timing Ref. Voltages | 1.5V       | 0.8V and 2V  |

Figure 6. AC Testing Input Output Waveform

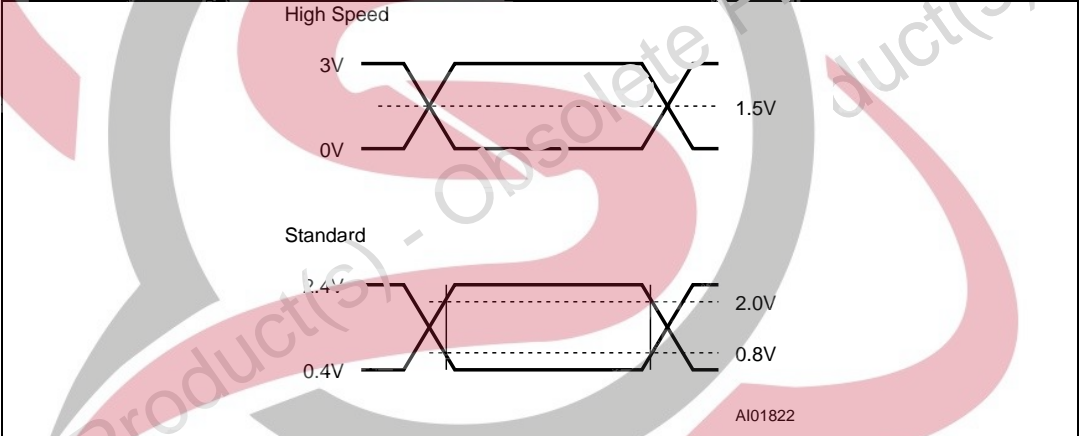
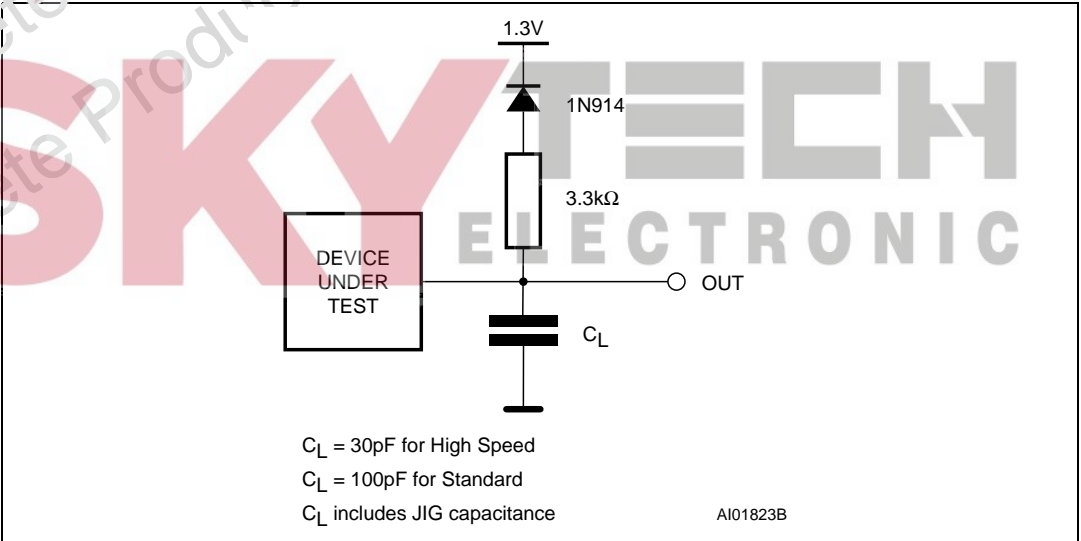


Figure 7. AC Testing Load Circuit



$T_A = 0 \text{ to } 70 \text{ }^{\circ}\text{C}$  or  $-40 \text{ to } 85 \text{ }^{\circ}\text{C}$ ;  $V_{CC} = 5V \pm 5\%$  or  $5V \pm 10\%$ ;  $V_{PP} = V_{CC}$

**Table 9. Read Mode AC Characteristics <sup>(1)</sup> (-50 and -70)**

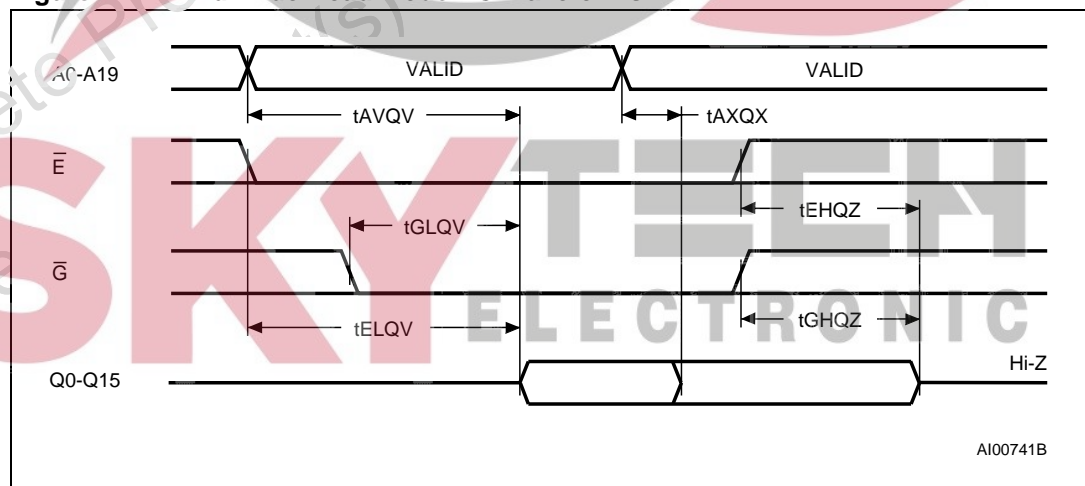
| Symbol                           | Alt              | Parameter                               | Test Condition                                 | M27C160            |      |                    |      | Unit |
|----------------------------------|------------------|---|--|--------------------|------|--------------------|------|------|
|                                  |                  |   |  | -50 <sup>(2)</sup> |      | -70 <sup>(2)</sup> |      |      |
|                                  |                  |   |  | Min.               | Max. | Min.               | Max. |      |
| t <sub>AVQV</sub>                | t <sub>ACC</sub> | Address Valid to Output Valid           | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ |                    | 50   |                    | 70   | ns   |
| t <sub>BHQV</sub>                | t <sub>ST</sub>  | BYTE High to Output Valid               | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ |                    | 50   |                    | 70   | ns   |
| t <sub>ELQV</sub>                | t <sub>CE</sub>  | Chip Enable Low to Output Valid         | $\overline{G} = V_{IL}$                        |                    | 50   |                    | 70   | ns   |
| t <sub>GLQV</sub>                | t <sub>OE</sub>  | Output Enable Low to Output Valid       | $\overline{E} = V_{IL}$                        |                    | 30   |                    | 35   | ns   |
| t <sub>BLQZ</sub> <sup>(3)</sup> | t <sub>STD</sub> | BYTE Low to Output Hi-Z                 | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ |                    | 30   |                    | 30   | ns   |
| t <sub>EHQZ</sub> <sup>(3)</sup> | t <sub>DF</sub>  | Chip Enable High to Output Hi-Z         | $\overline{G} = V_{IL}$                        | 0                  | 25   | 0                  | 25   | ns   |
| t <sub>GHQZ</sub> <sup>(3)</sup> | t <sub>DF</sub>  | Output Enable High to Output Hi-Z       | $\overline{E} = V_{IL}$                        | 0                  | 25   | 0                  | 25   | ns   |
| t <sub>AXQX</sub>                | t <sub>OH</sub>  | Address Transition to Output Transition | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ | 5                  |      | 5                  |      | ns   |
| t <sub>BLQX</sub>                | t <sub>OH</sub>  | BYTE Low to Output Transition           | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ | 5                  |      | 5                  |      | ns   |

1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
2. Speed obtained with High Speed AC measurement conditions.
3. Sampled only, not 100% tested.

**Table 10. Read Mode AC Characteristics<sup>(1)</sup> (-90, -100, -120 and -150)**

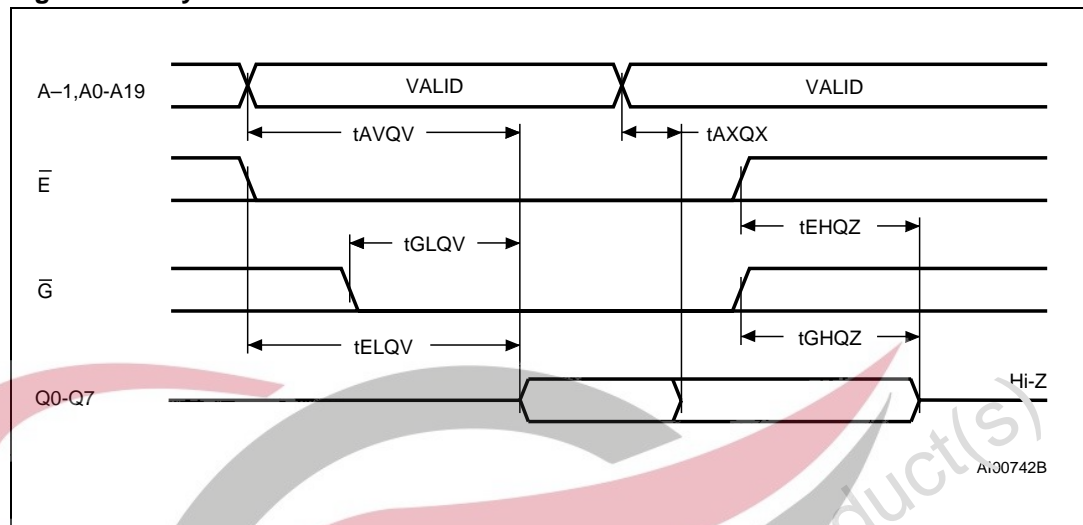
| Symbol                           | Alt              | Parameter                               | Test Condition                                      | M27C160            |      |                     |      |                          |      | Unit |
|----------------------------------|------------------|---|---|--------------------|------|---------------------|------|--------------------------|------|------|
|                                  |                  |   |   | -90 <sup>(2)</sup> |      | -100 <sup>(2)</sup> |      | -120/-150 <sup>(2)</sup> |      |      |
|                                  |                  |   |   | Min.               | Max. | Min.                | Max. | Min.                     | Max. |      |
| t <sub>AVQV</sub>                | t <sub>ACC</sub> | Address Valid to Output Valid           | $\overline{E} = V_{IL},$<br>$\overline{G} = V_{IL}$ |                    | 90   |                     | 100  |                          | 120  | ns   |
| t <sub>BHQV</sub>                | t <sub>ST</sub>  | BYTE High to Output Valid               | $\overline{E} = V_{IL},$<br>$\overline{G} = V_{IL}$ |                    | 90   |                     | 100  |                          | 120  | ns   |
| t <sub>ELQV</sub>                | t <sub>CE</sub>  | Chip Enable Low to Output Valid         | $\overline{G} = V_{IL}$                             |                    | 90   |                     | 100  |                          | 120  | ns   |
| t <sub>GLQV</sub>                | t <sub>OE</sub>  | Output Enable Low to Output Valid       | $\overline{E} = V_{IL}$                             |                    | 45   |                     | 50   |                          | 60   | ns   |
| t <sub>BLQZ</sub> <sup>(3)</sup> | t <sub>STD</sub> | BYTE Low to Output Hi-Z                 | $\overline{E} = V_{IL},$<br>$\overline{G} = V_{IL}$ |                    | 30   |                     | 40   |                          | 50   | ns   |
| t <sub>EHQZ</sub> <sup>(3)</sup> | t <sub>DF</sub>  | Chip Enable High to Output Hi-Z         | $\overline{G} = V_{IL}$                             | 0                  | 30   | 0                   | 40   | 0                        | 50   | ns   |
| t <sub>GHQZ</sub> <sup>(3)</sup> | t <sub>DF</sub>  | Output Enable High to Output Hi-Z       | $\overline{E} = V_{IL}$                             | 0                  | 30   | 0                   | 40   | 0                        | 50   | ns   |
| t <sub>AXQX</sub>                | t <sub>OH</sub>  | Address Transition to Output Transition | $\overline{E} = V_{IL},$<br>$\overline{G} = V_{IL}$ | 5                  |      | 5                   |      | 5                        |      | ns   |
| t <sub>BLQX</sub>                | t <sub>OH</sub>  | BYTE Low to Output Transition           | $\overline{E} = V_{IL},$<br>$\overline{G} = V_{IL}$ | 5                  |      | 5                   |      | 5                        |      | ns   |

1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
2. Speed obtained with High Speed AC measurement conditions.
3. Sampled only, not 100% tested.

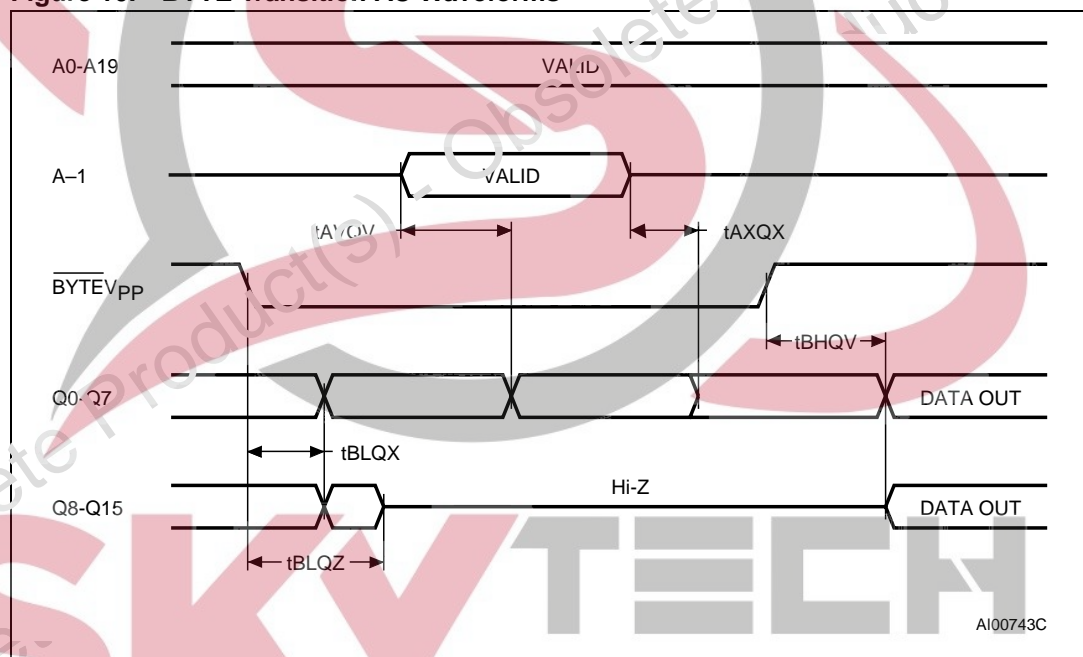
**Figure 8. Word-Wide Read Mode AC Waveforms**

Note:  $\overline{BYTE}V_{PP} = V_{IH}$ .

Figure 9. Byte-Wide Read Mode AC Waveforms



Note:  $\overline{BYTEV}_{PP} = V_{IL}$ .

Figure 10.  $\overline{BYTE}$  Transition AC Waveforms

Note: Chip Enable ( $\overline{E}$ ) and Output Enable ( $\overline{G}$ ) =  $V_{IL}$ .

$T_A = 25\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$ ;  $V_{PP} = 12.5\text{V} \pm 0.25\text{V}$

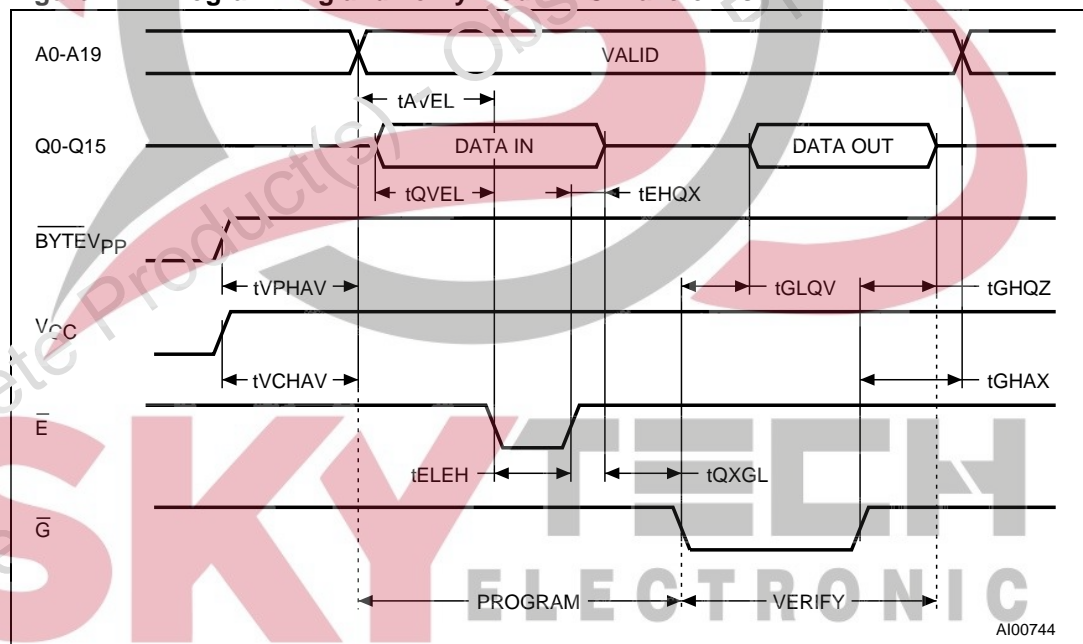
**Table 11. Programming Mode AC Characteristics<sup>(1)</sup>**

| Symbol                  | Alt       | Parameter                                | Test Condition | Min | Max | Unit          |
|-------------------------|-----------|--|----------------|-----|-----|---------------|
| $t_{A\text{VEL}}$       | $t_{AS}$  | Address Valid to Chip Enable Low         |                | 2   |     | $\mu\text{s}$ |
| $t_{Q\text{VEL}}$       | $t_{DS}$  | Input Valid to Chip Enable Low           |                | 2   |     | $\mu\text{s}$ |
| $t_{V\text{PHAV}}$      | $t_{VPS}$ | $V_{PP}$ High to Address Valid           |                | 2   |     | $\mu\text{s}$ |
| $t_{V\text{CHAV}}$      | $t_{VCS}$ | $V_{CC}$ High to Address Valid           |                | 2   |     | $\mu\text{s}$ |
| $t_{E\text{LEH}}$       | $t_{PW}$  | Chip Enable Program Pulse Width          |                | 45  | 55  | $\mu\text{s}$ |
| $t_{E\text{HQX}}$       | $t_{DH}$  | Chip Enable High to Input Transition     |                | 2   |     | $\mu\text{s}$ |
| $t_{Q\text{XGL}}$       | $t_{OES}$ | Input Transition to Output Enable Low    |                | 2   |     | $\mu\text{s}$ |
| $t_{G\text{LQV}}$       | $t_{OE}$  | Output Enable Low to Output Valid        |                |     | 120 | ns            |
| $t_{G\text{HQZ}}^{(2)}$ | $t_{DFP}$ | Output Enable High to Output Hi-Z        |                | 0   | 130 | ns            |
| $t_{G\text{HAX}}$       | $t_{AH}$  | Output Enable High to Address Transition |                | 0   |     | ns            |

1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

2. Sampled only, not 100% tested.

**Figure 11. Programming and Verify Modes AC Waveforms**





## 5 Package mechanical data

### 5.1 42-pin Ceramic Frit-seal DIP with window (FDIP42WB)

Figure 12. FDIP42WB package outline

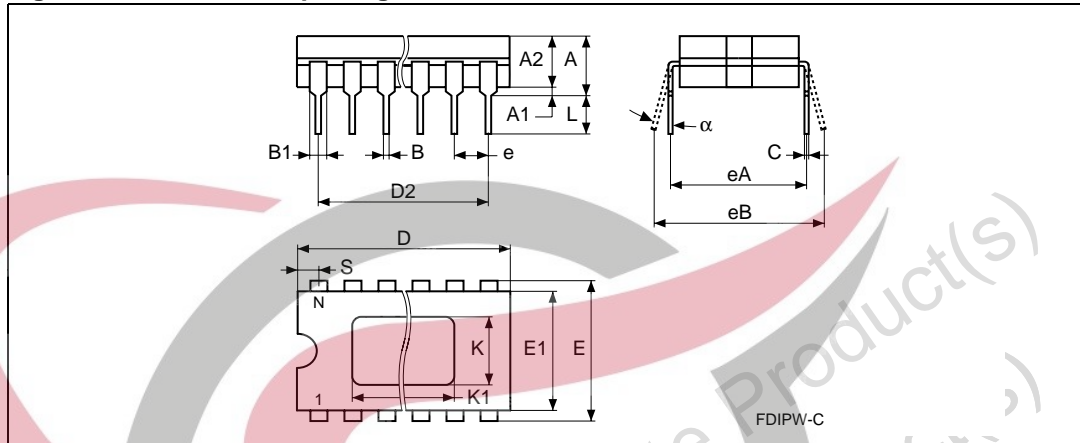


Table 12. FDIP42WB package mechanical data

| Symbol | millimeters |       |       | inches |       |       |
|--------|-------------|-------|-------|--------|-------|-------|
|        | Min.        | Typ.  | Max.  | Min.   | Typ.  | Max.  |
| A      |             |       | 5.71  |        |       | 0.225 |
| A1     | 0.50        |       | 1.78  | 0.020  |       | 0.070 |
| A2     | 3.90        |       | 5.08  | 0.154  |       | 0.200 |
| B      | 0.40        |       | 0.55  | 0.016  |       | 0.022 |
| B1     | 1.27        |       | 1.52  | 0.050  |       | 0.060 |
| C      | 0.22        |       | 0.31  | 0.009  |       | 0.012 |
| D      |             |       | 54.81 |        |       | 2.158 |
| D2     |             | 50.80 |       |        | 2.000 |       |
| E      |             | 15.24 |       |        | 0.600 |       |
| E1     | 14.50       |       | 14.90 | 0.571  |       | 0.587 |
| e      | 2.29        |       | 2.79  | 0.090  |       | 0.110 |
| eA     | 15.40       |       | 15.80 | 0.606  |       | 0.622 |
| eB     | 16.17       |       | 18.32 | 0.637  |       | 0.721 |
| K      | 9.32        |       | 9.47  | 0.367  |       | 0.373 |
| K1     | 11.30       |       | 11.55 | 0.445  |       | 0.455 |
| L      | 3.18        |       | 4.10  | 0.125  |       | 0.161 |
| S      | 1.52        |       | 2.49  | 0.060  |       | 0.098 |
| α      | 4°          |       | 15°   | 4°     |       | 15°   |
| N      |             | 42    |       |        | 42    |       |

# 5.2 42-pin Plastic DIP, 600 mils width (PDIP42)

Figure 13. PDIP42 package outline

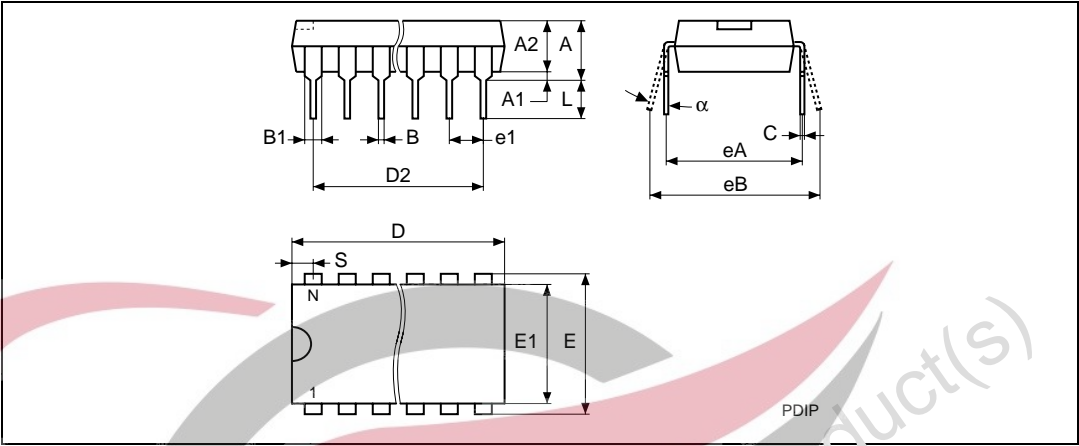


Table 13. PDIP42 package mechanical data

| Symbol   | millimeters |       |       | inches |       |       |
|----------|-------------|-------|-------|--------|-------|-------|
|          | Min.        | Typ.  | Max.  | Min.   | Typ.  | Max.  |
| A        |             |       | 5.08  |        |       | 0.200 |
| A1       | 0.25        |       |       | 0.010  |       |       |
| A2       | 3.56        |       | 4.06  | 0.140  |       | 0.160 |
| B        | 0.38        |       | 0.53  | 0.015  |       | 0.021 |
| B1       | 1.27        |       | 1.65  | 0.050  |       | 0.065 |
| C        | 0.20        |       | 0.36  | 0.008  |       | 0.014 |
| D        | 52.20       |       | 52.71 | 2.055  |       | 2.075 |
| D2       |             | 50.80 |       |        | 2.000 |       |
| E        |             | 15.24 |       |        | 0.600 |       |
| E1       | 13.59       |       | 13.84 | 0.535  |       | 0.545 |
| e1       |             | 2.54  |       |        | 0.100 |       |
| eA       |             | 14.99 |       |        | 0.590 |       |
| eB       | 15.24       |       | 17.78 | 0.600  |       | 0.700 |
| L        | 3.18        |       | 3.43  | 0.125  |       | 0.135 |
| S        | 0.86        |       | 1.37  | 0.034  |       | 0.054 |
| $\alpha$ | 0°          |       | 10°   | 0°     |       | 10°   |
| N        |             | 42    |       |        | 42    |       |

### 5.3 42-lead Shrink Plastic DIP, 600 mils width (SDIP42)

Figure 14. SDIP42 package outline

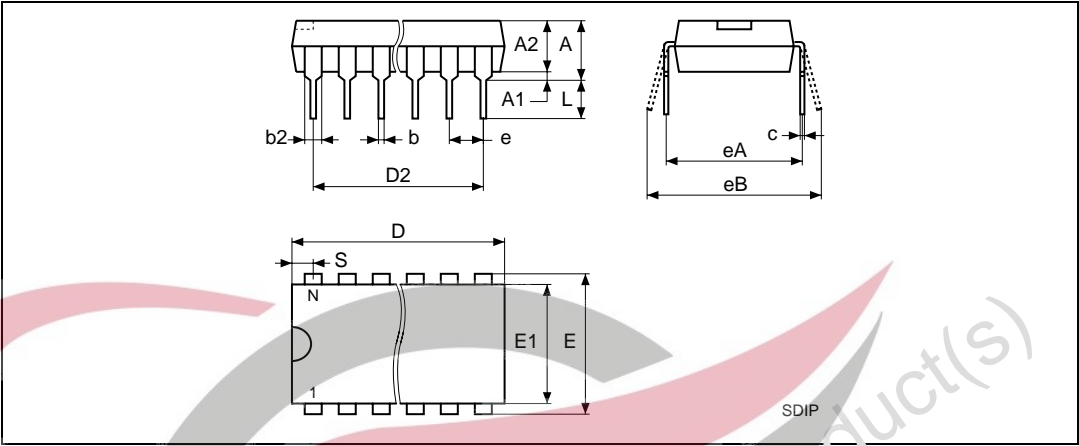


Table 14. SDIP42 package mechanical data

| Symbol | millimeters |       |       | inches |       |       |
|--------|-------------|-------|-------|--------|-------|-------|
|        | Min.        | Typ.  | Max.  | Min.   | Typ.  | Max.  |
| A      |             |       | 5.08  |        |       | 0.200 |
| A1     | 0.51        |       |       | 0.020  |       |       |
| A2     | 3.05        | 3.81  | 4.57  | 0.120  | 0.150 | 0.180 |
| b      | 0.38        | 0.46  | 0.56  | 0.015  | 0.018 | 0.022 |
| b2     | 0.89        | 1.02  | 1.14  | 0.035  | 0.040 | 0.045 |
| c      | 0.23        | 0.25  | 0.38  | 0.009  | 0.010 | 0.015 |
| D      | 36.50       | 36.83 | 37.08 | 1.440  | 1.450 | 1.460 |
| D2     |             | 35.60 |       |        | 1.402 |       |
| e      |             | 1.78  |       |        | 0.070 |       |
| E      | 15.24       |       | 16.00 | 0.600  |       | 0.630 |
| E1     | 12.70       | 13.72 | 14.48 | 0.500  | 0.540 | 0.570 |
| eA     |             | 15.24 |       |        | 0.600 |       |
| eB     |             |       | 18.54 |        |       | 0.730 |
| L      | 2.54        | 3.30  | 3.56  | 0.100  | 0.130 | 0.140 |
| S      |             | 0.64  |       |        | 0.025 |       |
| N      |             | 42    |       |        | 42    |       |

# 5.4 44-lead Square Plastic Leaded Chip Carrier (PLCC44)

Figure 15. PLCC44 package outline

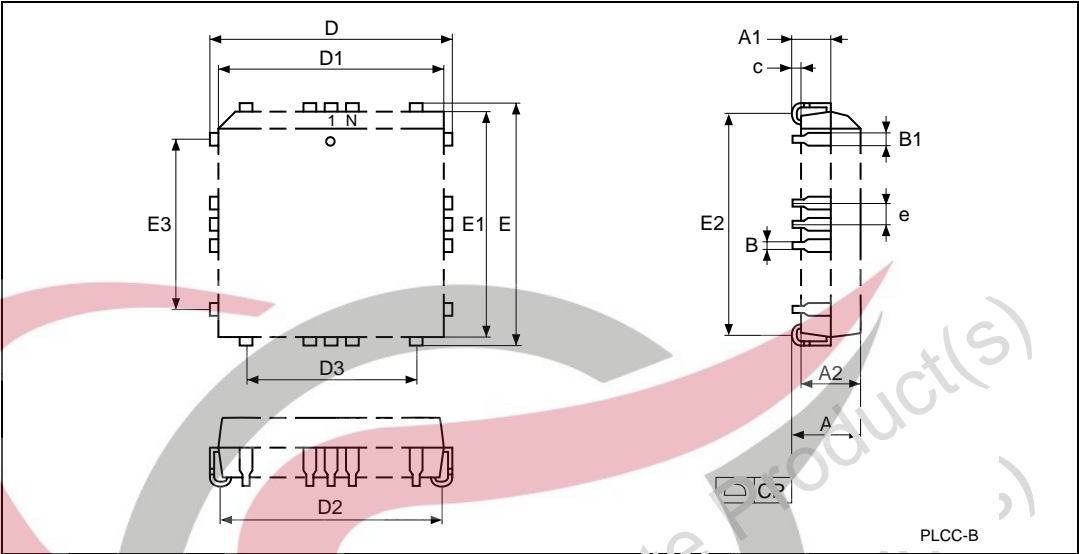


Table 15. PLCC44 package mechanical data

| Symbol | millimeters |        |        | inches |        |        |
|--------|-------------|--------|--------|--------|--------|--------|
|        | Min.        | Typ.   | Max.   | Min.   | Typ.   | Max.   |
| A      | 4.200       |        | 4.570  | 0.1654 |        | 0.1799 |
| A1     | 2.290       |        | 3.040  | 0.0902 |        | 0.1197 |
| A2     | 3.650       |        | 3.700  | 0.1437 |        | 0.1457 |
| B      | 0.351       |        | 0.533  | 0.0130 |        | 0.0210 |
| B1     | 0.361       |        | 0.812  | 0.0260 |        | 0.0320 |
| C      |             |        | 0.101  |        |        | 0.0040 |
| c      |             | 0.510  |        |        | 0.0201 |        |
| D      | 17.400      |        | 17.650 | 0.6850 |        | 0.6949 |
| D1     | 16.510      |        | 16.662 | 0.6500 |        | 0.6560 |
| D2     | 14.990      |        | 16.000 | 0.5902 |        | 0.6299 |
| D3     |             | 12.700 |        |        | 0.5000 |        |
| E      | 17.400      |        | 17.650 | 0.6850 |        | 0.6949 |
| E1     | 16.510      |        | 16.660 | 0.6500 |        | 0.6559 |
| E2     | 14.990      |        | 16.000 | 0.5902 |        | 0.6299 |
| E3     |             | 12.700 |        |        | 0.5000 |        |
| e      |             | 1.270  |        |        | 0.0500 |        |
| N      |             | 44     |        |        | 44     |        |

## 5.5 44-lead Plastic Small Outline, 525 mils body width (SO44)

Figure 16. SO44 package outline

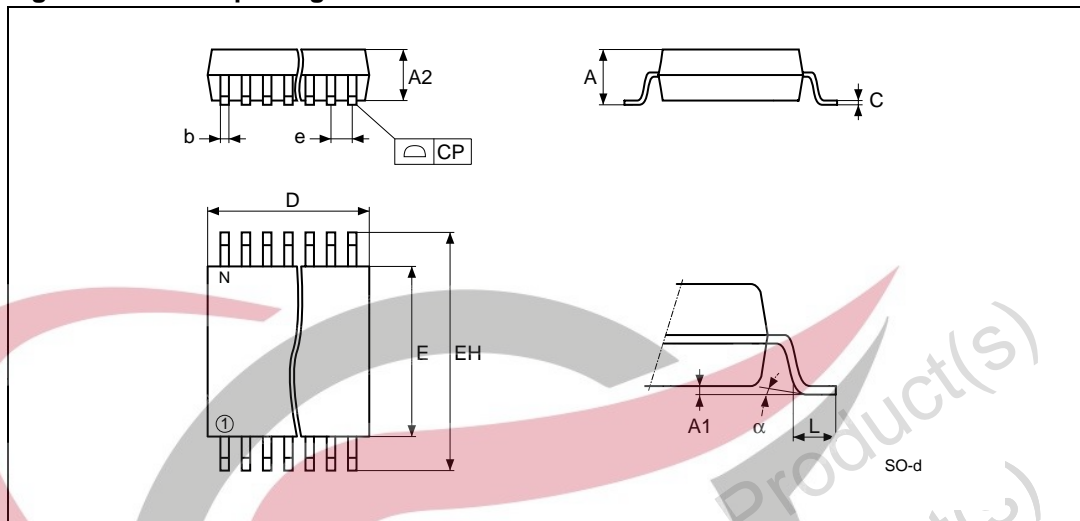


Table 16. SO44 package mechanical data

| Symbol | millimeters |       |       | inches |        |        |
|--------|-------------|-------|-------|--------|--------|--------|
|        | Min.        | Typ.  | Max.  | Min.   | Typ.   | Max.   |
| A      |             |       | 2.80  |        |        | 0.1102 |
| A1     | 0.10        |       |       | 0.0039 |        |        |
| A2     | 2.20        | 2.30  | 2.40  | 0.0866 | 0.0906 | 0.0945 |
| b      | 0.35        | 0.40  | 0.50  | 0.0138 | 0.0157 | 0.0197 |
| C      | 0.10        | 0.15  | 0.20  | 0.0039 | 0.0059 | 0.0079 |
| CP     |             |       | 0.08  |        |        | 0.0030 |
| D      | 28.00       | 28.20 | 28.40 | 1.1024 | 1.1102 | 1.1181 |
| E      | 13.20       | 13.30 | 13.50 | 0.5197 | 0.5236 | 0.5315 |
| EH     | 15.75       | 16.00 | 16.25 | 0.6201 | 0.6299 | 0.6398 |
| e      |             | 1.27  |       |        | 0.0500 |        |
| L      |             | 0.80  |       |        | 0.0315 |        |
| α      |             |       | 8°    |        |        | 8°     |
| N      |             | 44    |       |        | 44     |        |



## 6 Part numbering

**Table 17. Ordering Information Scheme**

Example:

|                                     |         |     |   |   |   |
|-------------------------------------|---------|-----|---|---|---|
|                                     | M27C160 | -70 | X | M | 1 |
| <b>Device Type</b>                  |         |     |   |   |   |
| M27                                 |         |     |   |   |   |
| <b>Supply Voltage</b>               |         |     |   |   |   |
| C = 5V                              |         |     |   |   |   |
| <b>Device Function</b>              |         |     |   |   |   |
| 160 = 16 Mbit (2mb x 8 or 1Mb x 16) |         |     |   |   |   |
| <b>Speed</b>                        |         |     |   |   |   |
| -50 <sup>(1)</sup> = 50 ns          |         |     |   |   |   |
| -70 <sup>(1)</sup> = 70 ns          |         |     |   |   |   |
| -90 = 90 ns                         |         |     |   |   |   |
| -100 = 100 ns                       |         |     |   |   |   |
| -120 = 120 ns                       |         |     |   |   |   |
| -150 = 150 ns                       |         |     |   |   |   |
| <b>V<sub>CC</sub> Tolerance</b>     |         |     |   |   |   |
| blank = ± 10%                       |         |     |   |   |   |
| X = ± 5%                            |         |     |   |   |   |
| <b>Package</b>                      |         |     |   |   |   |
| F = FC-P42V1                        |         |     |   |   |   |
| B = PDIF-42                         |         |     |   |   |   |
| S = SDIP42                          |         |     |   |   |   |
| K = PLCC44                          |         |     |   |   |   |
| M = SO44                            |         |     |   |   |   |
| <b>Temperature Range</b>            |         |     |   |   |   |
| 1 = 0 to 70 °C                      |         |     |   |   |   |
| 6 = -40 to 85 °C                    |         |     |   |   |   |

1. High Speed, see AC Characteristics section for further information.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

## 7 Revision history

**Table 18. Document revision history**

| Date         | Revision | Changes  |
|--------------|----------|--|
| January 1999 | 1        | First Issue  |
| 20-Sep-00    | 2        | AN620 Reference removed  |
| 19-Jul-01    | 3        | SDIP42 package added   |
| 17-Jan-02    | 4        | 50ns speed class added, SO44 package mechanical data and drawing clarified         |
| 12-Apr-2006  | 5        | Converted to new template. Updated ECOPACK® information. Removed Tape & Reel info. |

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